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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,577	12/04/2003	Chen-Jung Tsai	0941-0874P	5109

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,577	TSAI ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

a. In re claim 15, the limitation, "wherein the non-active surface of the first chip remains exposed" does not further limit the limitation from claim 10, "with the non-active surface of the first chip ... exposed beyond the encapsulation." The dependent claim is broader than the independent claim and thus is objected to for being in improper form.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 15 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. In re claims 15 and 16, the phrase "when the outer leads are attached to an exterior device," is not disclosed in the specification, nor is such claim language inferred from reading pp. 7, lines 9-27, as indicated by Applicant in pp. 11 of applicant's remarks dated 06/23/05. On the contrary, the specification language is limited to the exposure of the non-active surface outside the encapsulant. The reason given by applicant in this section is not to attach the leads to an exterior device. Rather, the reason given by applicant for this embodiment is to enhance the heat-dissipation feature of the invention.

b. Therefore, the phrase, "when the outer leads are attached to an exterior device" constitutes new matter and is not given patentable weight in the instant application.

c. Further, the language is precatory in nature, not specifically claiming a structure, but rather expressing what *could* happen when the outer leads are so connected. The claim language then tends to recite the "intended use" of the proposed invention. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art. For this reason as well, the cited phrase is not given patentable weight regarding the final structure of the claimed invention.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 18 and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Shim (US 2004/0061202 A1).

In re claim 18, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface (within the encapsulant) and an opposing wire non-connecting surface (outside of the encapsulant).

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface

consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of the wires electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation (40) covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

In re claim 20, Shim discloses the device of claim 18, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation. The limitation, "and the wire non-connecting surface ... to an exterior device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device, therefore is not given patentable weight in this claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. (US 2004/0061202 A1) in view of Vaiyapuri (U.S. Patent No. 6,541,846 B2).

In re claim 1, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads;

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads.

Shim does not expressly disclose the first and second chips adhering to either surface of the same parts of the chip paddle. Vaiyapuri (esp. Figs. 1h) discloses first (130) and second (120) chips adhering to either surface of the same parts of the chip paddle (116). It would have been obvious for one skilled in the art at the time of the

invention to align the chips of Shim as disclosed by Vaiyapuri for the purpose, for example, of increasing the integrated circuit density of the semiconductor package device (Vaiyapuri; column 2, lines 51-57).

In re claim 2, Shim in view of Vaiyapuri discloses the device of claim 1, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[1].

In re claim 3, Shim in view of Vaiyapuri discloses the device of claim 1, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 4, Shim in view of Vaiyapuri discloses the device of claim 1, wherein the wires are metal lines.

In re claim 5, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads;

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[1] Note that Shim discloses this layer to comprise a "resin" but does not expressly disclose the conductive properties of the resin. That an epoxy resin such as used by Shim is insulative is well known in the prior art as taught by Oda et al. (U.S. Patent No. 6,489,668 B1; column 5, lines 23-30).

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with the second bonding pad and the leads; and

an encapsulation (40) covering the lead frame, the first chip, the second chip and the wires.

Shim does not expressly disclose the first and second chips adhering to either surface of the same parts of the chip paddle. Vaiyapuri (esp. Figs. 1h) discloses first (130) and second (120) chips adhering to either surface of the same parts of the chip paddle (116). It would have been obvious for one skilled in the art at the time of the invention to align the chips of Shim as disclosed by Vaiyapuri for the purpose, for example, of increasing the integrated circuit density of the semiconductor package device (Vaiyapuri; column 2, lines 51-57).

In re claim 6, Shim in view of Vaiyapuri discloses the device of claim 5, wherein each lead further comprises an inner lead covered by the encapsulation and outer lead extending beyond the encapsulation.

In re claim 7, Shim in view of Vaiyapuri discloses the device of claim 5, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[2].

In re claim 8, Shim in view of Vaiyapuri discloses the device of claim 5, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 9, Shim in view of Vaiyapuri discloses the device of claim 5, wherein the wires are metal lines.

In re claim 19, Shim does not expressly disclose the first and second chips adhering to either surface of the same parts of the chip paddle. Vaiyapuri (esp. Figs. 1h) discloses first (130) and second (120) chips adhering to either surface of the same parts of the chip paddle (116). It would have been obvious for one skilled in the art at the time of the invention to align the chips of Shim as disclosed by Vaiyapuri for the purpose, for example, of increasing the integrated circuit density of the semiconductor package device (Vaiyapuri; column 2, lines 51-57).

8. Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shim as applied to claim 10 above, and further in view of Wu et al. (US 2003/0214048 A1).

[2] Note that Shim discloses this layer to comprise a "resin" but does not expressly disclose the conductive properties of the resin. That an epoxy resin such as used by Shim is insulative is well known in the prior art as taught by Oda et al. (U.S. Patent No. 6,489,668 B1; column 5, lines 23-30).

In re claim 10, Shim (esp. Fig. 1) discloses a dual chips stacked packaging structure, comprising:

a first chip (26), having an active surface and an opposing non-active surface, the active surface consisting of a central area and peripheral area having a plurality of first bonding pads;

a lead frame (18), comprising a plurality of leads and a chip paddle (15) having a first adhering surface (at resin 28) and second adhering surface (at resin 32), the first adhering surface adhered the active surface of the first chip in such way to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface (within the encapsulant) and an opposing wire non-connecting surface (outside of the encapsulant).

a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads; and

a plurality of wires (34, 36), wherein parts of the wires electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of the wires electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation (40) covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

Shim does not expressly disclose the non-active surface of the first chip being exposed from the encapsulant. Wu (esp. Fig. 6) discloses the non-active surface (351) of a first chip (35) being exposed from the encapsulant. It would have been obvious for one skilled in the art at the time of the invention to expose the first chip of Shim as disclosed by Wu for the purpose, for example, of improving the heat-dissipating efficiency of the semiconductor device package structure (Wu; section [0029], lines 10-14).

The limitation, "when the outer leads ... device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device,

In re claim 11, Shim in view of Wu discloses the device of claim 10, wherein each lead (18) further comprises an inner lead (20) covered by the encapsulation and outer lead extending beyond the encapsulation.

In re claim 12, Shim in view of Wu discloses the device of claim 10, wherein the first adhering surface of the chip paddle and the active surface of the first chip are adhered by a non-conductive solid or liquid adhesive[3].

In re claim 13, Shim in view of Wu discloses the device of claim 10, wherein the second adhering surface of the chip paddle and the non-active surface of the second chip are connected by a solid or liquid adhesive (resin 32).

In re claim 14, Shim in view of Wu discloses the device of claim 10, wherein the wires are metal lines.

In re claim 15, Shim in view of Wu discloses the device of claim 11, wherein the non-active surface of the first chip remains exposed.

The limitation, "when the outer leads ... device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device, therefore is not given patentable weight in this claim.

In re claim 16, Shim in view of Wu discloses the device of claim 11, wherein the wire non-connecting surface of the leads remains exposed. The limitation, "when the outer leads ... device" is a recitation of the intended use of the claimed invention and does not further describe the structure of the device, therefore is not given patentable weight in this claim.

9. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shim/Wu as applied to claim 10 above, and further in view of Vaiyapuri (US 6,541,846 B2).

In re claim 17, Shim discloses the device of claim 10, but does not expressly disclose the first and second chips adhering to either surface of the same parts of the chip paddle. Vaiyapuri (esp. Figs. 1h) discloses first (130) and second (120) chips adhering to either surface of the same parts of the chip paddle (116). It would have been obvious for one skilled in the art at the time of the invention to align the chips of Shim as disclosed by Vaiyapuri for the purpose, for example, of increasing the integrated circuit density of the semiconductor package device (Vaiyapuri; column 2, lines 51-57).

Response to Arguments

9. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. Applicant's amendments to claims 1, 5 and 10, as well as the addition of new claims 15-20, necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

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[3] Note that Shim discloses this layer to comprise a "resin" but does not expressly disclose the conductive properties

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815

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of the resin. That an epoxy resin such as used by Shim is insulative is well known in the prior art as taught by Oda et al. (U.S. Patent No. 6,489,668 B1; column 5, lines 23-30).

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER